A GaAs DOUBLE-BALANCED DUAL-GATE FET MIXER IC FOR UHF RECEIVER FRONT-END APPLICATIONS

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ABSTRACT

A double-balanced dual-gate FET mixer has been developed aiming at the application to a front-end circuit of the UHF receivers.

An experimental IC has exhibited a 6 − 8 dB conversion gain without matching over a wide frequency range from 100 MHz to 800 MHz with the well suppressed RF/LO feedthough by more than 20 dB and third-order intermodulation product of -60 dB.

INTRODUCTION

Implementation of the front-end circuit of the TV tuner is an attractive goal in applying GaAs analog IC's to the consumer area (1). In order to reach this goal many efforts have been devoted so for mainly dealing with low noise wide band amplifier circuits and mixer circuits.

Although the wide band amplifier circuits have made a considerable progress recently[2 − 3], little achievement has been attained as for the mixer circuits.

This paper describes a work undertaken to design, fabricate and test the GaAs double-balanced dual-gate FET mixer IC for use in a front-end circuit of the UHF receivers.

DESIGN

A particular target that we aimed at is:
1) conversion gain: >5 dB
2) RF/LO feedthrough: <-20 dB
3) third-order intermodulation: <-55 dB.

A double-balanced and dual-gate configuration was used for the present monolithic circuit design. The reasons are that the double-balanced configuration is essential for suppressing the RF/LO feedthrough and the dual-gate structure is suitable for avoiding cumbersome passive couplers.

An analitical calculation of the conversion gain [4] of the dual-gate FET was carried out by using a simple model——cascode connection of two single-gate FET's ——[5]. In Fig. 1, are shown the calculated results of the conversion gain as a function of the gate width Wg for the different Source/Load impedances Z_S and Z_L. The principal

single-gate FET parameters used in the calculation are:
source resistance; $2.4 \times 10^3/Wg \; [\Omega/\mu m]$
gate resistance; $1.7 \times 10^{-2} \times Wg \; [\Omega \cdot \mu m]$
drain conductance; $6.7 \times 10^{-6} \times Wg \; [S \cdot \mu m]$
gate-source capacitance; $1.3 \times 10^{-3} \times Wg \; [pF \cdot \mu m]$.
Despite designing the Source/Load impedances to be 50Ω is desirable for practical applications, the result of Fig. 1 indicates that use of 50Ω requires a large gate width Wg in order to satisfy the target conversion gain of 5 dB resulting in the increased power consumption and chip size. Therefore, we designed Source/Load impedances to be $Z_S = Z_L = 200\Omega$ which requests use of the 1:4 balun. The calculated result of the conversion gain for $Z_S = Z_L = 200\Omega$ informs that the target of 5 dB conversion gain can be satisfied by taking Wg=300 μm.

The circuit diagram of the monolithic mixer IC is shown in Fig. 2. The RF and LO signals are applied to the first and second gates, respectively through the baluns. The IF signal is taken out also through the balun.
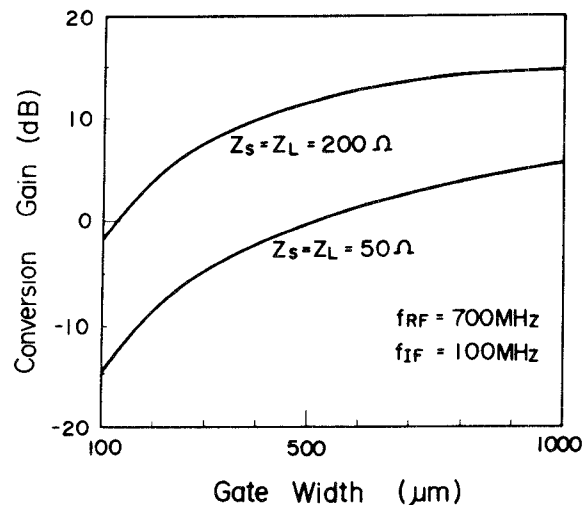

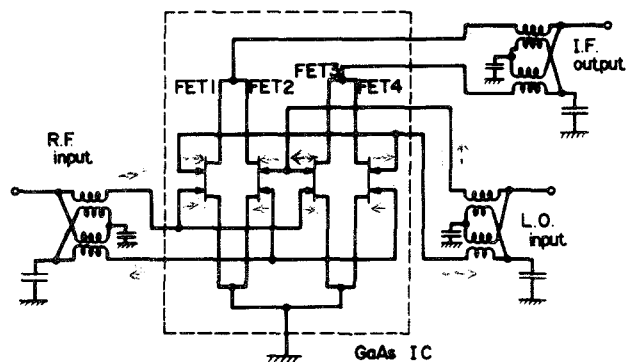Fig. 1.   Calculated conversion gain as a function of the gate width.

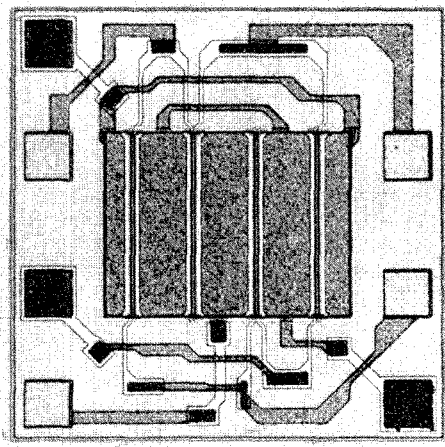Fig. 2. Circuit diagram of the monolithic mixer IC.

Fig. 4. Conversion gain of the experimental IC as a function of the RF frequency.

Fig. 3. Photograph of the completed mixer IC.

Fig. 5. Conversion gain of the experimental IC as a function of the LO power.

FABRICATION

The full ion-implantation process was used to fabricate the device. The n-type active and n^+-type contact layers were provided by selective ion implantation of Si onto an undoped LEC GaAs substrate under the condition of 5×10^{12} cm^{-2} dose at 130 KeV and 5×10^{13} cm^{-2} dose at 150 KeV, respectively. AuGe/Ni/Au and Ti/Al were used for the Ohmic contacts and the Schottky gate, respectively. The gate width of each FET was 300 μm as previously mentioned and the gate length was 1 μm. A photograph of the completed mixer IC is shown in Fig. 3. The chip size is 750 μm x 750 μm.

TEST RESULTS

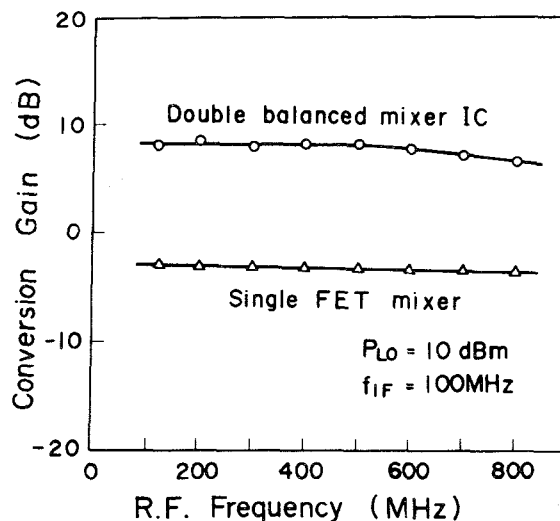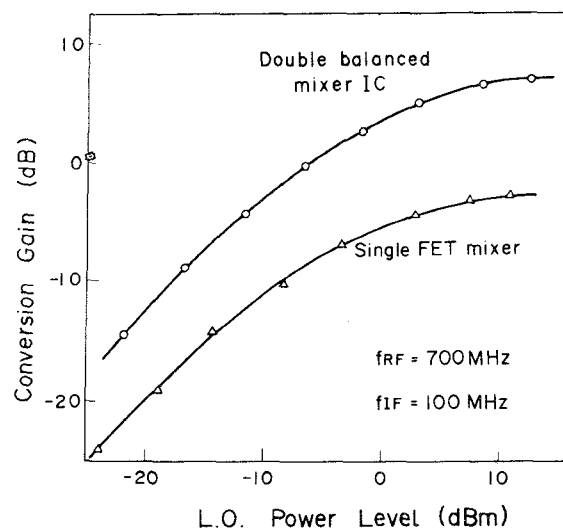In Fig. 4, is shown the conversion gain of the experimental IC as a function of the RF

frequency. The IF frequency is fixed to be 100 MHz. RF and LO levels are -20 dBm and 10 dBm, respectively. The results of the single FET mixer with the same dimension are also shown in Fig. 4 for comparison. Fig. 5 shows the conversion gain as a function of the LO power. It is found that the experimental device exhibits a very high conversion gain of 6 - 8 dB over a wide frequency range from 100 MHz to 800 MHz being very close to the values predicted by the design theory shown in Fig. 1. It is also noted that these high conversion gain is attained without additional matching circuits.
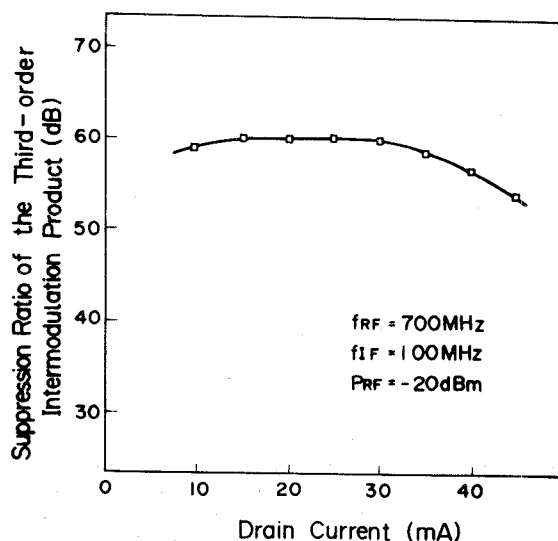
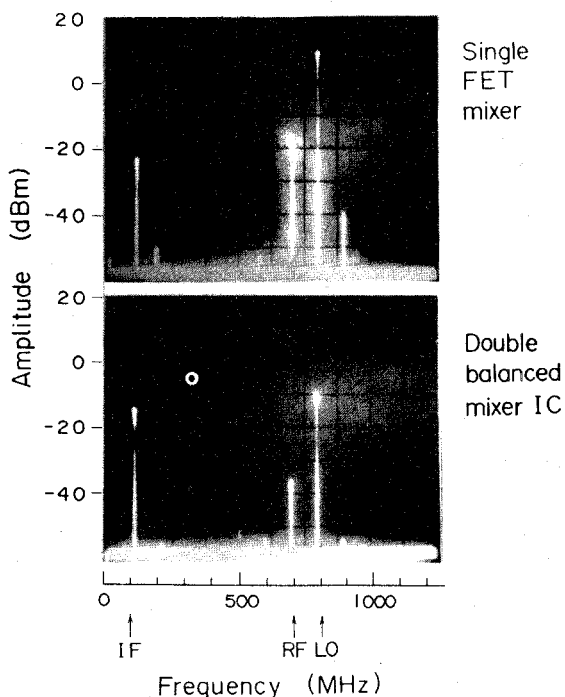Fig. 6. Suppression ratio of the third-order intermodulation product as a function of the drain current.

The measured suppression ratio of the third-order intermodulation product IM_3 is shown in Fig. 6 where the RF signal at 700 MHz and the interference signal at 701 MHz are both -20 dBm and LO signal is 10 dBm. It is seen that the IM_3 at 101 MHz is as high as 60 dB up to approximately 30 mA of the drain current.

The output frequency spectrum are shown in Fig. 7 comparing with that of the single FET mixer. It is obvious in this photograph that the RF and LO feedthrough's are well suppressed by more than 20 dB.

CONCLUSION

It is shown that the GaAs monolithic double-balanced dual-gate mixer IC has been developed, for the first time, exhibiting 6 - 8 dB conversion gain without matching over a wide frequency range from 100 MHz to 800 MHz with the extremely suppressed feedthrough and the intermodulation products.

ACKNOWLEDGMENT

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Fig. 7. Output frequency spectrum of the oxperimental IC comparing with that of the single FET mixer; P_{LO} = 10 dBm, P_{RF}=-20 dBm.